A832-4X4-66T2 DRAM SIMM FPM

8MX32 DRAM SIMM using 4MX4, 2K Refresh, 5V

GENERAL DESCRIPTION

The Advantage A832-4X4-66T2 is a 8MX32 Dynamic RAM high-density memory module. The Advantage A832-4X4-66T2 consists of eight CMOS 4MX4 bit DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The A832-4X4-66T2 is a Single In-line Memory Module with edge connections and is intended for mounting into 72-pin edge connectors sockets.

FEATURES

- Part Identification
  A832-4X4-66T2
- Fast Page Mode Operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V+/- 10% power supply
- JEDEC standard PDPin & pinout
- PCB: **Height(1.000mil)**, single sided component

PIN CONFIGURATIONS (Front/Back)

1	Vss	29	A11	57	DQ12
2	DQ0	30	Vcc	58	DQ28
3	DQ16	31	A8	59	Vcc
4	DQ1	32	A9	60	DQ29
5	DQ17	33	Res(RAS1)	61	DQ13
6	DQ2	34	RAS0	62	DQ30
7	DQ18	35	NC	63	DQ14
8	DQ3	36	NC	64	DQ31
9	DQ19	37	NC	65	DQ15
10	Vcc	38	NC	66	NC
11	NC	39	Vss	67	PD1
12	A0	40	CAS0	68	PD2
13	A1	41	CAS2	69	PD3
14	A2	42	CAS3	70	PD4
15	A3	43	CAS1	71	NC
16	A4	44	RAS0	72	Vss
17	A5	45	Res(RAS1)		
18	A6	46	NC		
19	A10	47	W		
20	DQ4	48	NC		
21	DQ20	49	DQ8		
22	DQ5	50	DQ24		
23	DQ21	51	DQ9		
24	DQ6	52	DQ25		
25	DQ22	53	DQ10		
26	DQ7	54	DQ26		
27	DQ23	55	DQ11		
28	A7	56	DQ27		

PIN NAMES

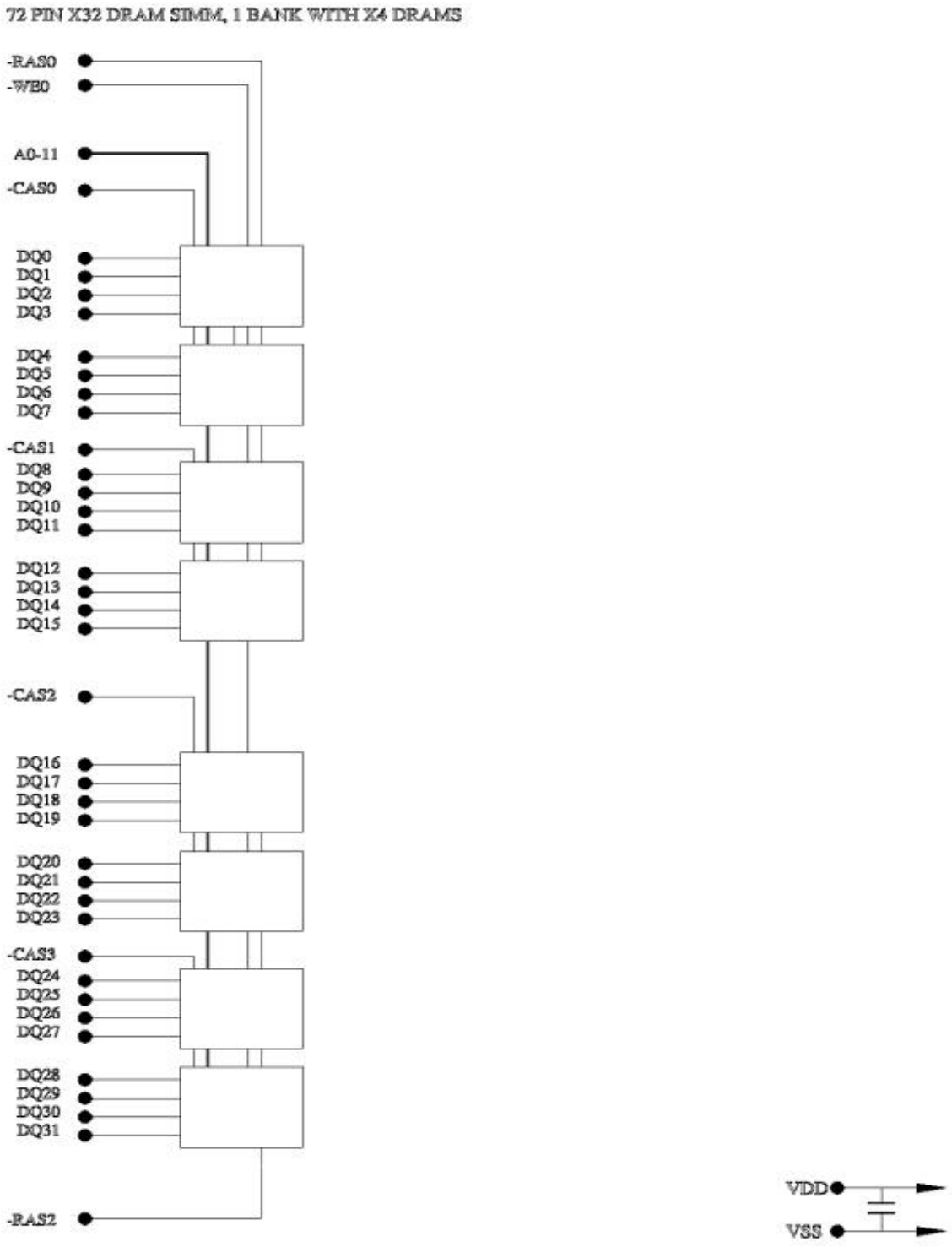
A0 ~ A11	Address inputs(4K)
A0~A10	Address Inputs(2K)
DQ0~DQ31	Data input/output
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$~$\overline{CAS3}$	Col. address strobe
PD1~PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

*These pins are not used on this module
**These pins should be NC in the system that does not support SPD

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
$\overline{RAS}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
$\overline{CAS}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
W	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, WE active.
DQ0 ~ DQ31	input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 7.0	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 7.0	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended o condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	2.0	0	0	V
Input high voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}
*2 : -2.0V/20ns, Pulse width is measured at Vss

CAPACITANCE (V_{cc} = 5V, T_A = 25°C, f = 1MHz)

Pin	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C_{IN1}	-	100	pF
Input capacitance[W]	C_{IN2}	-	130	pF
Input capacitance[RAS0]	C_{IN3}	-	70	pF
Input capacitance[CAS0-CAS3]	C_{IN4}	-	30	pF
Input/Output capacitance[DQ0-31]	C_{DQ1}	-	20	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Speed	A832-4X4-66T2 Min	Max	Unit
Operating current	I_{CC1}	-50 -60	- -	896 816	mA
Standby Current	I_{CC2}	Don't care	-	32	mA
$\overline{RAS}$ Only Refresh Current	I_{CC3}	-50 -60	- -	896 816	mA
EDO Mode Current	I_{CC4}	-50 -60	- -	736 656	mA
Standby Current	I_{CC5}	Don't care	-	16	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	-50 -60	- -	896 816	mA
Input Leakage Current	I_{IL}	Don't care	-40	80	uA
Output Leakage Current	I_{OL}	Don't care	-5	10	uA
Output High Voltage Level	V_{OH}	Don't care	2.4	-	V
Output Low Voltage Level	V_{OL}	Don't care	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=W=V_{IH})
I_{CC3} : RAS Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=W=Vcc-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0<V_{IN}<Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current (Data Out is disabled, 0V<V_{OUT}<Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

***NOTE**: I_{CC1},I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

AC CHARACTERISTICS

Parameter	Symbol	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Note
Random read or write cycle time	t_{RC}	90		110		ns	1
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	1
Access time from column address	t_{AA}		25		30	ns	1
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		us	
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	0	13	0	15	ns	1
Transition time(rise and fall)	t_{tT}	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	1
Row address set-up time	t_{ASR}	0		0		ns	1
Row address hold time	t_{RAH}	10		10		ns	4
Column address set-up time	t_{ASC}	0		0		ns	5
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	4
Read command set-up time	t_{RCS}	0		0		ns	5
Read command hold time referenced to $\overline{CAS}$	t_{RAL}	0		0		ns	3
Read command hold time referenced to $\overline{RAS}$	t_{RCH}	0		0		ns	3
Write command hold time	t_{RRH}	10		10		ns	3
Write command pulse width	t_{WCH}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{WP}	13		15		ns	2
Write command to $\overline{CAS}$ lead time	t_{RWL}	13		15		ns	
Data-in set-up time	t_{CWL}	0		0		ns	
Data-in hold time	t_{DS}	10		15		ns	
Refresh period (4K Ref)	t_{DH}		64		64	ms	
Refresh period (2K Ref)	t_{REF}		32		32	ms	
Write command set-up time	t_{REF}	0		0		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before_$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to CAS precharge time	t_{RPC}	5		5		ns	
$\overline{CAS}$ precharge time (C-B-R counter test)	t_{CPT}	20		20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	
Hyper page mode cycle time	t_{HPC}	35		40		ns	
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	5		5		ns	
W to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
W to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	0		0		ns	
Output buffer turn off delay from W	t_{WEZ}	0		0		ns	
W to data delay	t_{WED}	15		15		ns	
W pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	

Notes

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before Proper device operation is achieved.

2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring Timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively bt t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t_{WCS}>(min), t_{WCS}>(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameter are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the W leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures That t_{RAC}(max) can be met. T_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If RAS goes to high before $\overline{CAS}$ high going, the open circuit condition of the ouput is achieved by CAS high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}>t_{CP} min

Engineering Drawing