EDC1672-8X8-66VNBS4 DRAM DIMM

16MX72 Nonbuffered EDO DIMM based on 8MX8, 4K Refresh, 3.3V DRAMs

GENERAL DESCRIPTION

The Advantage EDC1672-8X8-66VNBS4 is a JEDEC standard 16MX72 bit Dynamic RAM high density memory module. The Advantage EDC1672-8X8-66VNBS4 consists of eighteen CMOS 16mx4 TSOP-II 400mil, EDO Mode DRAM mounted on a 168-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The EDC1672-8X8-66VNBS4 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

FEATURES

Row Access Time	60ns
Column Access Time	17ns
Random Read/Write Cycle Time	104ns
Page Mode Cycle Time	25ns
Refresh Type	CAS before RAS (CBR), RAS only, Hidden Refresh
Refresh Rate	4096 cycles in 64ms
Access Cycle	EDO PAGE MODE
Height	(1,150mil)

PIN CONFIGURATIONS (FRONT/BACK)

1	V_{SS}	22	CB1	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	CB5	127	V_{SS}	148	V_{SS}
2	DQ0	23	V_{SS}	44	OE2	65	DQ21	86	DQ32	107	V_{SS}	128	RFU	149	DQ53
3	DQ1	24	NC	45	RAS2	66	DQ22	87	DQ33	108	NC	129	NC	150	DQ54
4	DQ2	25	NC	46	CAS2	67	DQ23	88	DQ34	109	NC	130	CAS6	151	DQ55
5	DQ3	26	V_{DD}	47	CAS3	68	V_{SS}	89	DQ35	110	V_{DD}	131	CAS7	152	V_{SS}
6	V_{DD}	27	WE0	48	WE2	69	DQ24	90	V_{DD}	111	RFU	132	RFU	153	DQ56
7	DQ4	28	CAS0	49	V_{DD}	70	DQ25	91	DQ36	112	CAS4	133	V_{DD}	154	DQ57
8	DQ5	29	CAS1	50	NC	71	DQ26	92	DQ37	113	CAS5	134	NC	155	DQ58
9	DQ6	30	RAS0	51	NC	72	DQ27	93	DQ38	114	NC	135	NC	156	DQ59
10	DQ7	31	OE0	52	CB2	73	V_{DD}	94	DQ39	115	RFU	136	CB6	157	V_{DD}
11	DQ8	32	V_{SS}	53	CB3	74	DQ28	95	DQ40	116	V_{SS}	137	CB7	158	DQ60
12	V_{SS}	33	A0	54	V_{SS}	75	DQ29	96	V_{SS}	117	A1	138	V_{SS}	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V_{SS}	99	DQ43	120	A7	141	DQ50	162	V_{SS}
16	DQ12	37	A8	58	DQ19	79	NC	100	DQ44	121	A9	142	DQ51	163	NC
17	DQ13	38	A10	59	V_{DD}	80	NC	101	DQ45	122	A11	143	V_{DD}	164	NC
18	V_{DD}	39	NC	60	DQ20	81	NC	102	V_{DD}	123	NC	144	DQ52	165	SA0
19	DQ14	40	V_{DD}	61	NC	82	SDA	103	DQ46	124	V_{DD}	145	NC	166	SA1
20	DQ15	41	V_{DD}	62	RFU	83	SCL	104	DQ47	125	RFU	146	RFU	167	SA2
21	CB0	42	RFU	63	NC	84	V_{DD}	105	CB4	126	RFU	147	NC	168	V_{DD}

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45, 114, 129	RAS0-RAS3	Input	Row-Address Strobe: RAS is used to clock-in the row address bits. Two RAS inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0-CAS7	Input	Column-Address Strobe: CAS is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS inputs allow byte access control for any memory bank configuration.
27, 48	WE0, WE2	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31,44	OE0-OE2	Input	Output Enable: OE is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
21-22, 52-53, 105-106, 136-137	CB0-CB7	Input/ Output	Check Bits.
42, 62, 111, 115, 125-126, 128, 132, 146	RFU	-	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground
82	SDA	Input/ Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs. These pins are used to configure the presence-detect device.

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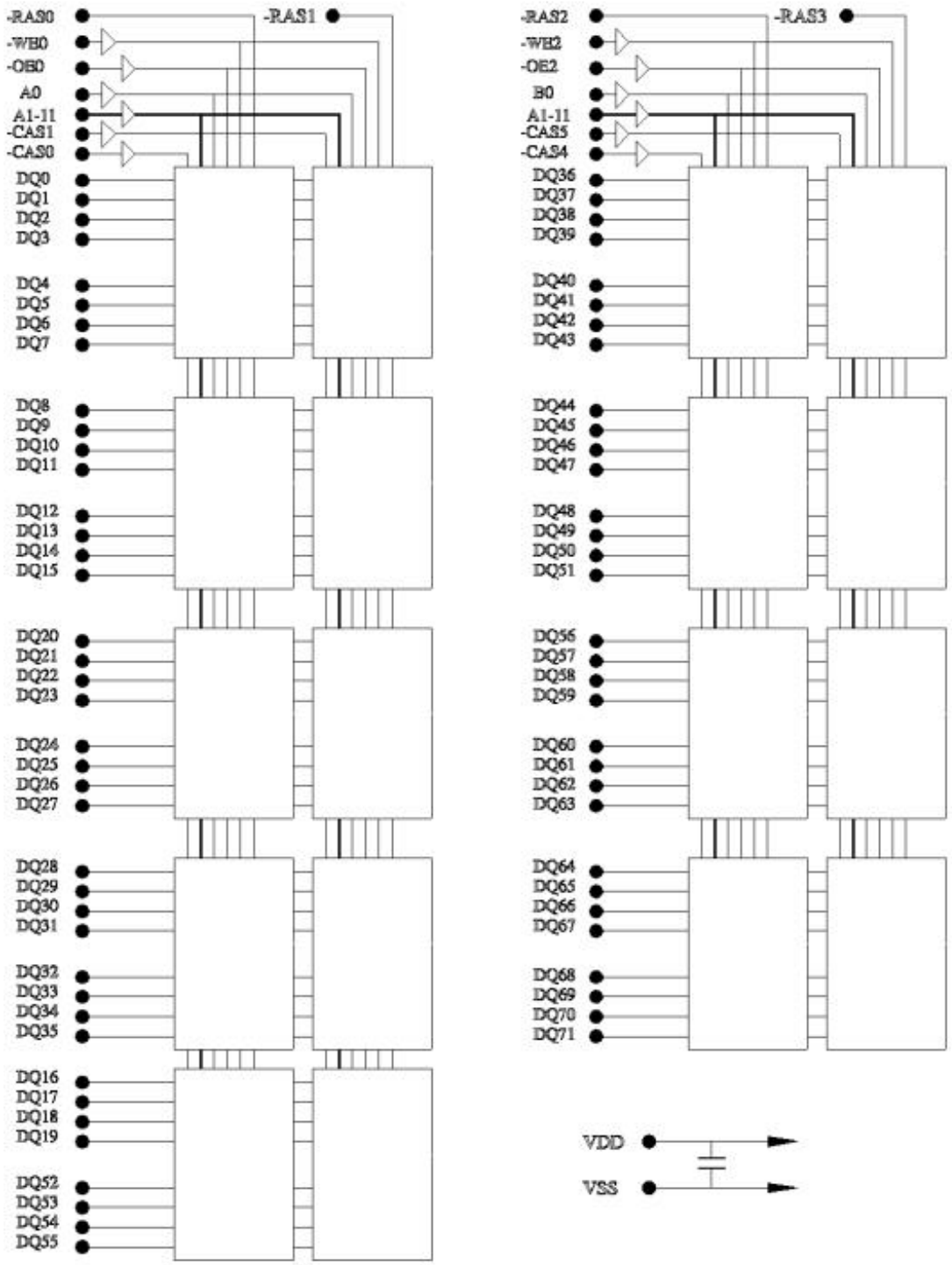
BLOCK DIAGRAM

168 PIN, X72 ECC DRAM DIMM, 2 BANKS WITH X8 DRAMs



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	
Voltage on VDD supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	
Storage temperature	T_{STG}	-55 ~ +125	
Short circuit current	I_{OS}	50	

DC OPERATING CONDITIONS

(V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	VCC	3	3.6	V
INPUT HIGH VOLTAGE	VIH	2	VDD +0.3	V
INPUT LOW VOLTAGE	VIL	-0.5	0.8	V
INPUT LEAKAGE CURRENT	I(IL)	-18	18	Ua
OUTPUT LEAKAGE CURRENT	I(OL)	-5	5	Ua

DC OPERATING CHARACTERISTICS

(V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
OPERATING CURRENT (RAS, CAS, Address cycling @t_{RC}=min)	I_{CC1}	-	2,880	mA
STANDBY CURRENT (RAS=CAS=VIH)	I_{CC2}	-	18	mA
RAS ONLY REFRESH CURRENT (CAS=VIH, RAS cycling @ t_{RC}=min)	I_{CC3}	-	2,880	mA
EDO PAGE MODE CURRENT (RAS=VIL, CAS cycling: t_{HPC}=min)	I_{CC4}	-	2,160	mA
STANDBY CURRENT (RAS=CAS=V_{CC}-0.2V)	I_{CC5}	-	9	mA
CAS BEFORE RAS REFRESH CURRENT (RAS and CAS cycling @t_{RC}=min)	I_{CC6}	-	2,160	mA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH}= -2mA)	V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL}= 2mA)	V_{OL}		0.4	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance [A0-A11]	C_{IN1}	-	96	pF
Input Capacitance [WE0, WE2,OE0, OE2]	C_{IN2}	-	67	pF
Input Capacitance [RAS0-RAS3]	C_{IN3}	-	67	pF
Input Capacitance [CAS0-CAS3]	C_{IN4}	-	46	pF
Input Capacitance [SCL, SA0-SA2]	C_{IN5}	-	6	pF
Input/Output capacitance [DQ0-DQ63, SDA]	C_{DQ}	-	22	pF

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AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Access time from column address	tAA		30	ns
Column-address setup to CAS precharge during writes	tACH	15		ns
Column-address hold time (referenced to RAS)	tAR	45		ns
Column-address setup time	tASC	0		ns
Row-address setup time	tASR	0		ns
Column address to WE delay time	tAWD	49		ns
Access time from CAS	tCAC		15	ns
Column-address hold time	tCAH	10		ns
CAS pulse width	tCAS	10	10,000	ns
CAS hold time (CBR Refresh)	tCHR	10		ns
CAS to output in Low-Z	tCLZ	0		ns
Data output hold after CAS LOW	tCOH	3		ns
CAS precharge time	tCP	10		ns
Access time from CAS precharge	tCPA		35	ns
CAS to RAS precharge time	tCRP	5		ns
CAS hold time	tCSH	45		ns
CAS setup time (CBR Refresh)	tCSR	5		ns
CAS to WE delay time	tCWD	35		ns
WRITE command to CAS lead time	tCWL	10		ns
Data-in hold time	tDH	10		ns
Data-in setup time	tDS	0		ns
Output disable	tOD	0	15	ns
Output enable	tOE		15	ns
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	10		ns
OE HIGH hold time from CAS HIGH	tOEHC	10		ns
OE HIGH pulse width	tOEP	5		ns
OE LOW to CAS HIGH setup time	tOES	5		ns
Output buffer turn-off delay	tOFF	0	15	ns
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		ns
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		ns
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	56		ns
Access time from RAS	tRAC		60	ns
RAS to column-address delay time	tRAD	12		ns
Row-address hold time	tRAH	10		ns
RAS pulse width (EDO PAGE MODE)	tRASP	60	125,000	ns
Random READ or WRITE cycle time	tRC	104		ns
RAS to CAS delay time	tRCD	14		ns
READ command hold time (referenced to CAS)	tRCH	0		ns
READ command setup time	tRCS	0		ns
Refresh period (4,096 cycles)			64	mss

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AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
RAS precharge time	tRP	40		ns
RAS to CAS precharge time	tRPC	5		ns
READ command hold time (referenced to RAS)	tRRH	0		ns
RAS hold time	tRSH	15		ns
READ-WRITE cycle time	tRWC	140		ns
RAS to WE delay time	tRWD	79		ns
WRITE command to RAS lead time	tRWL	15		ns
Transition time (rise or fall)	tT	2	50	ns
WRITE command hold time	tWCH	10		ns
WRITE command hold time (referenced to RAS)	tWCR	45		ns
WE command setup time	tWCS	0		ns
Output disable delay from WE (CAS HIGH)	tWHZ		15	ns
WRITE comand pulse width	tWP	5		ns
WE pulse width for output disable when CAS HIGH	tWRH	10		ns
WE holt time (CBR Refresh)	tWRP	10		ns
WE pulse width for output disable when CAS HIGH	tWPZ	10		ns

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NOTES

1. All voltages referenced to Vss.
2. This parameter Is sampled. VDD =+3.3V: f = I MHz.
3. Ice Is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range Is ensured.
6. An initial pause of *1*00**C**Ls is required after power-up, followed by eight RAS# REFRESH cycles (RAS*-ONLY or CBR with WE* HIGH), before proper device operation Is ensured. The eight RAS# cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume tT = 2ns.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. .In addition to meeting the transition rate specification, all Input signals must transit between VIH and VIL (or between VIL and VIH) In a monotonic manner.
10. lfCAS# and RAS# = V IH, data output is High-Z.
11. If CAS# = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and lOOpF and VOL = 0.8V and VOH = 2V.
13. Requires that *-*AA* and 'CAC are not violated.
14. Requires that tAA and 'RAC are not violated.
15. lfCAS* Is LOW at the falling edge ofRAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ICP.
16. The tRCD (MAX) limit Is no longer specified. tRCD (MAX) was specified as a reference point only. If tRCD was greater than the specified tRCD (MAX) limit, then access time was controlled exclusively by tCAC (tRAC [MIN] no longer applied). With or without the tRCD (MAX) limit, tAA and tCAC must always be met.
17. The tRAD (MAX) limit Is no longer specified. tRAD (MAX) was specified as a reference point only. If 'RAD was greater than the specified tRAD (MAX) limit, then access time was controlled exclusively by fAA (tRAC and *CAC no longer applied). With or without the tRAD (MAX) limit, tAA, tRAC and 'CAC must always be met.
18. Either 'RCH or tRRH must be satisFied for a READ cycle.
19. tOFF (MAX) defines the time at which the output achieves the open circuit condition and Is not referenced to VOH or VOL.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE* = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. tWCS, tRWD, tAWD and 'CWD are not restrictive operating parameters. *WCS applies to EARLY WRITE cycles. If WCS > tWCS (MIN), the cycle Is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. tRWD, tAWD and tCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying Input data. OE# held HIGH and WE# taken LOW after CAS* goes LOW result In a LATE WRITE (OE#-controlled) cycle. 'WCS, tRWD, tCWD and <AWD are not applicable In a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design,
26. Measured with the specified current load and lOOpF.
27. 'OFF on an EDO module is determined by the latter of the RAS# and CAS* signals to transition HIGH.
28. The SPD EEPROM WRITE cycle time CWR) is the time from a valid stop condition of a write sequence to the end of the EEPROM Internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. All other Inputs at 0.2V or VDD - 0.2V.
31. VIH overshoot: VIH (MAX) = VDD +2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate.

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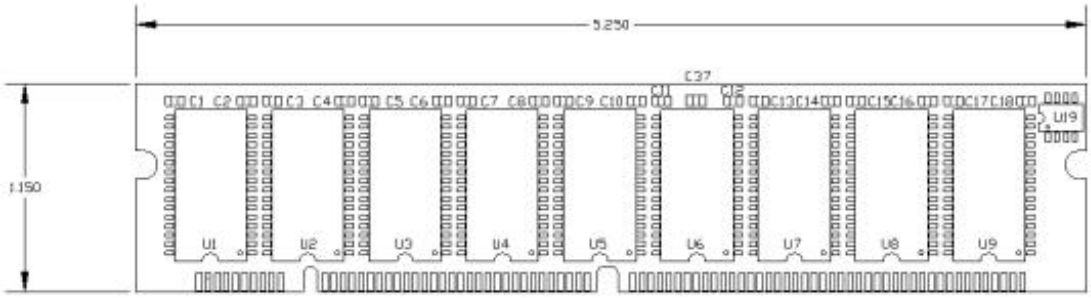
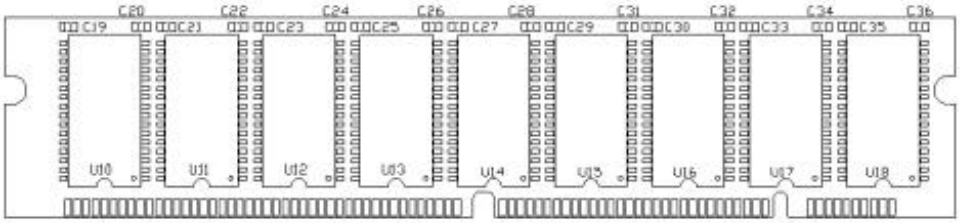
ENGINEERING DRAWING





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