SD1672-8X8-84VS4C2 SDRAM DIMM

16MX72 SDRAM DIMM based on 8MX8, 4Banks, 4K Refresh, 3.3V DRAMs with SPD

GENERAL DESCRIPTION

The Advantage SD1672-8X8-84VS4C2 is a 16MX72 Synchronous Dynamic RAM high density memory module. The Advantage SD1672-8X8-84VS4C2 consists of eighteen CMOS 8MX8 bit with 4 Internal Banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The SD1672-8X8-84VS4C2 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance range
  Max. Freq. (Speed): 100 MHz (10ns @ CL=2)
- Burst mode operation
- Auto and Self refresh capability(4096 Cycles)
- LVTTL compatible inputs and outputs
- Single 3.3V+/- 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1,2,4,8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB: **Height (1.300mil)**

PIN CONFIGURATIONS (Front/Back)

1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1*	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

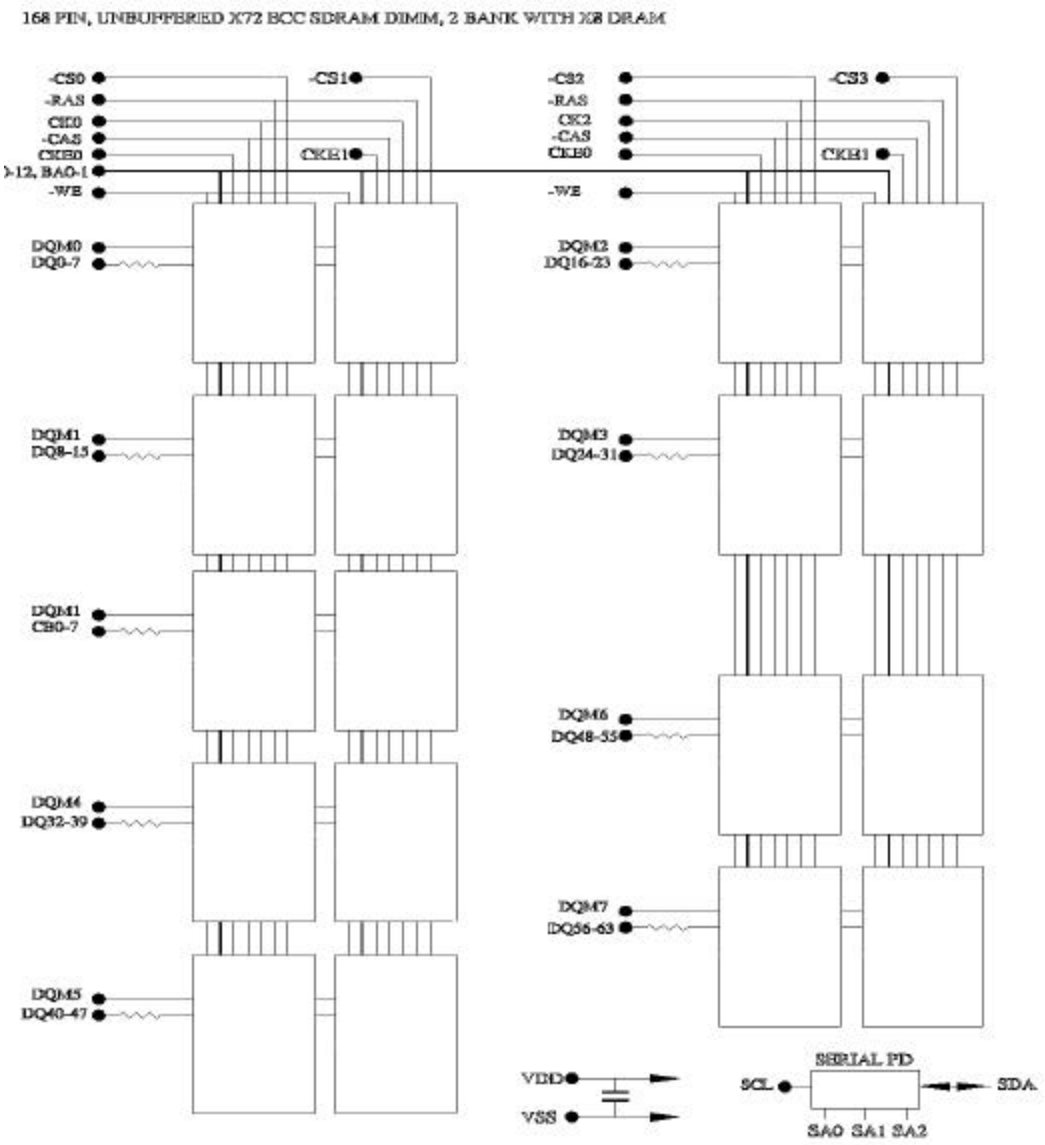
A0 ~ A11	Address input
BA0 ~ BA1	Select bank
DQ0~DQ63	Data input/output
CB0 ~ 7	Check bit
CLK0~CLK3	Clock input
CKE0~CKE1	Clock enable input
CS0~CS3	Chip select input
RAS	Row address strobe
CAS	Col. address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply
VSS	Ground
*VREF	Power for ref.
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	SPD Address
WP	Write protection
DU	Don't use

*These pins are not used on this module
**These pins should be NC in the system that does not support SPD

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
CS	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to VSS through 47KW Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be wirte-protected.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	W
Short circuit current	I_{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.5	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage (Inputs)	I_{IL}	2.4	-	18	uA	3
Input leakage (I/O pins)	I_{IL}	-	-	3	uA	3,4

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is £ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is £ 3ns.
3. Any input 0V £ V_{IN} £ V_{DDQ}. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V £ V_{OUT} £ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C_{ADD}	49	70	pF
RAS, CAS, WE	C_{IN}	49	70	pF
CKE (CKE0 ~ CKE1)	C_{CKE}	25	50	pF
Clock (CLK0 ~ CLK3)	C_{CLK}	15	25	pF
CS (CS0 ~ CS3)	C_{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	9	18	pF
DQ (DQ0 ~ DQ63)	C_{OUT1}	10	20	pF
CB (CB0 ~ CB7)	C_{OUT2}	10	15	pF

DC CHARACTERISTICS

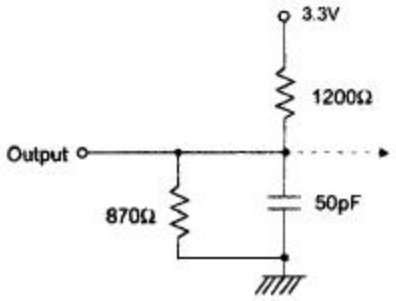
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version –10E	Unit	Note
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq T_{RC}$ (min) I_{OL} = 0 mA		1,170	mA	1
Precharge standby current	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		36	mA	3
Precharge standby current	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		36	mA	3
Precharge standby current	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		270	mA	4
Precharge standby current	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		126	mA	4
Active standby current	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		90	mA	3
Active standby current	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		90	mA	3
Active standby current	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		540	mA	4,5
Active standby current	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		360	mA	4,5
Operating Current	I_{CC4}	I_{OL} = 0 mA Page burst	CL=3	1,080	mA	1,6
		2Banks activated t_{CCD} = 2CLKs	CL=2	1,080	mA	1,6
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,025	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V		18	mA	

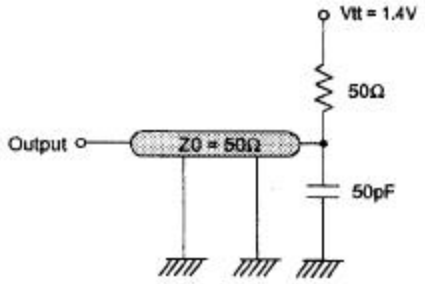
1. Measured with outputs open
2. Refresh period 64ms
3. Power-power mode
4. Non-power-down mode
5. One bank active
6. Burst mode

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

Parameter	Symbol	Version –10E	Unit	Note
Row active to row active delay	t_{RRD}(min)	20	ns	1
RAS to CAS delay	t_{RCD}(min)	20	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	50	ns	1
Row active time	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	70	ns	1
Last data in to row precharge	t_{RDL}(min)	1	CLK	2
Last data in to new col. address delay	t_{CDL}(min)	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Col. address to col. address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data CL=3		2	each	4
Number of valid output data CL=2		1	each	4

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
CLK cycle time CL=3	t_{CC}	10	1000	ns	1
CLK cycle time CL=2	t_{CC}	10	1000	ns	1
CLK to valid ouput delay	t_{SAC}		6	ns	4
CLK to valid ouput delay	t_{SAC}		6	ns	5
Output data hold time	t_{OH}e	3		ns	4
Output data hold time	t_{OH}e	3		ns	5
CLK high pulse width	t_{CH}	3		ns	3
CLK low pulse width	t_{CL}	3		ns	3
Input setup time	t_{SS}	2		ns	3
Input hold time	t_{SH}	1		ns	3
CLK to output in Low-Z	t_{SLZ}	1		ns	2
CLK to output to Hi-Z	t_{SHZ}		6	ns	4
CLK to output to Hi-Z	t_{SHZ}		6	ns	5

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns. If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. CL=3
5. CL=2

Command			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11,A9-A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0-A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0-A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

1. OP Code : Operand code A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state. A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Mechanical Specification